

The listing of claims will replace all prior versions, and listings, of claims in the application.

**Listing of Claims:**

1. An edge termination structure for a silicon carbide semiconductor device, comprising:
  - a plurality of spaced apart concentric floating guard rings in a silicon carbide layer that at least partially surround a silicon carbide-based semiconductor junction;
  - an insulating layer on the floating guard rings; and
  - a silicon carbide surface charge compensation region between the floating guard rings and adjacent the insulating layer.
2. The edge termination structure of Claim 1, wherein the floating guard rings extend a first distance into the silicon carbide layer and the surface charge compensation region extends a second distance into the silicon carbide layer, the second distance being less than the first distance.
3. The edge termination structure of Claim 1, wherein the surface charge compensation region is lighter doped than the guard rings.
4. The edge termination structure of Claim 1, wherein the surface charge compensation region extends completely between adjacent ones of the floating guard rings.
5. The edge termination structure of Claim 1, wherein the surface charge compensation region extends between adjacent ones of the floating guard rings but does not extend completely between two adjacent floating guard rings.
6. The edge termination structure of Claim 1, wherein the surface charge compensation region comprises implanted regions in the silicon carbide layer.

7. The edge termination structure of Claim 1, wherein the surface charge compensation region comprises a plurality of surface charge compensation regions.

8. The edge termination structure of Claim 1, wherein the surface charge compensation region comprises a single region that overlaps the floating guard rings.

9. The edge termination structure of Claim 1, wherein the surface charge compensation region comprises a second silicon carbide layer on the silicon carbide layer.

10. The edge termination structure of Claim 1, wherein the surface charge compensation region has a dopant concentration such that the surface of the surface charge compensation region adjacent the oxide layer is partially depleted by surface charges of the oxide layer and fully depleted when a reverse bias is applied to the device.

11. The edge termination structure of Claim 1, wherein the surface charge compensation region has a dose charge of from about  $1 \times 10^{12}$  to about  $7 \times 10^{12} \text{ cm}^{-2}$ .

12. The edge termination structure of Claim 1, wherein the surface charge compensation region extends a distance of from about 0.1  $\mu\text{m}$  to about 2.0  $\mu\text{m}$  into the silicon carbide layer.

13. The edge termination structure of Claim 1, wherein the surface charge compensation region does not extend completely between two adjacent floating guard rings and to provide a gap of from about 0.1  $\mu\text{m}$  to about 2.0  $\mu\text{m}$  between the surface charge compensation region and one of the two adjacent floating guard rings.

14. The edge termination structure of Claim 1, wherein the floating guard rings are uniformly spaced, non-uniformly spaced and/or combinations of uniformly and non-uniformly spaced.

15. The edge termination structure of Claim 1, wherein the guard rings extend from about 0.1  $\mu\text{m}$  to about 2.0  $\mu\text{m}$  into the silicon carbide layer.

16. The edge termination structure of Claim 1, wherein the guard rings have a spacing of from about 0.1  $\mu\text{m}$  to about 10  $\mu\text{m}$ .

17. The edge termination structure of Claim 1, wherein the plurality of floating guard rings comprises from about 2 to about 100 guard rings.

18. The edge termination structure of Claim 1, wherein the guard rings extend a distance of from about 2  $\mu\text{m}$  to about 1 mm from the semiconductor junction of the device.

19. The edge termination structure of Claim 1, wherein the floating guard rings have a dopant concentration of from about  $1 \times 10^{18} \text{ cm}^{-3}$  to about  $1 \times 10^{20} \text{ cm}^{-3}$ .

20. The edge termination structure of Claim 1, wherein the silicon carbide layer is an n-type silicon carbide layer and the guard rings and surface charge compensation region are p-type silicon carbide.

21. The edge termination structure of Claim 1, wherein the silicon carbide layer is a p-type silicon carbide layer and the guard rings and surface charge compensation region are n-type silicon carbide.

22.-41. Canceled.

42. An edge termination structure for a silicon carbide semiconductor device, comprising:

a plurality of spaced apart concentric floating guard rings in a silicon carbide layer that surround at least a portion of a silicon carbide-based semiconductor junction;

an insulating layer on the floating guard rings; and  
means for neutralizing effects of charges at an interface between the insulating layer and the silicon carbide layer in the region of the floating guard rings.

43. The edge termination structure of Claim 42, wherein the means for neutralizing comprises means for connecting adjacent guard rings when a maximum blocking voltage is not applied to the device and isolating adjacent guard rings when the maximum blocking voltage is applied to the device.

44. The edge termination structure of Claim 42, wherein the means for neutralizing comprises surface charge compensation regions between adjacent ones of the guard rings.

45. The edge termination structure of Claim 44, wherein an amount of charge in the surface charge compensation regions is small enough so that the surface charge compensation regions are depleted at a voltage lower than a blocking voltage of the device.

46. The edge termination structure of Claim 42, wherein the means for neutralizing comprises a surface charge compensation layer between adjacent ones of the guard rings.

47. The edge termination structure of Claim 46, wherein an amount of charge in the surface charge compensation layer is small enough so that the surface charge compensation layer is depleted at a voltage lower than a blocking voltage of the device.